REMARKS

Applicant hereby traverses the outstanding rejections and requests reconsideration and withdrawal in view of the remarks contained herein. Claims 1, 3 and 12 have been amended. Claims 1-27 are pending in this application.

Rejection under 35 U.S.C. § 102(e)

Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,675,324 to Marisetty et al. (hereinafter Marisetty).

It is well settled that to anticipate a claim, the reference must teach every element of the claim. *See* MPEP § 2131. Moreover, in order for a reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he elements must be arranged as required by the claim." *See* MPEP § 2131, citing *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990). Furthermore, in order for a reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* MPEP § 2131, citing *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913 (Fed. Cir. 1989). Applicants respectfully assert that the cited reference does not satisfy these requirements.

Claim 1, as amended, requires delaying to allow other cells associated with said partition to reach said initial rendezvous state. Claim 12, as amended, requires a processor to execute said partition instructions utilized to join said partition, and firmware device to store said partition instructions utilized to join said partition. Claim 21 requires transitioning to said partition state, by each cell. The Examiner has cited Marisetty as describing these limitations; Applicant respectfully disagrees with the Examiner's characterization of Marisetty.

Marisetty is directed to a multi-processor system that involves an error handling routine. When an error occurs (a parity error associated with the processor instruction cache), one of the processors is selected to execute an error handling routine defined in system firmware. The error handling routine causes the system to enter a rendezvous state. In the rendezvous state, one of the processors acts as a "monarch processor" to attempt to correct

the error. Col. 5, lines 48-50. The other processors enter a "spin-loop" or "idle state". Col. 6, lines 60-65. After correction of the error by the monarch processor, the system "exits the rendezvous state and all processors resume normal operations." Col. 5, lines 51-53.

With respect to claim 21, the Examiner has pointed to column 8, lines 51-64 as teaching transitioning to a partition state, by each cell. Applicant has carefully reviewed the section of Marisetty cited by the Examiner but can find no reference to transitioning to a partition state as required by claim 21. Instead the cited portion of Marisetty describes using either the SAL, PAL or monarch processor to correct a detected error and then sending, using the OS, a "wake up" signal to the slave processors.

Marisetty never describes delaying to allow other cells associated with said partition to reach said initial rendezvous state as required by claim 1, or a processor to execute said partition instructions utilized to join said partition, and firmware device to store said partition instructions utilized to join said partition as required by claim 12, or transitioning to said partition state, by each cell as required by claim 21. As Marisetty fails to describe at least these limitations of claims 1, 12 and 21, Applicant respectfully asserts that Marisetty does not teach each and every limitation of claims 1, 12 and 21 as required by §102.

Claims 2-11, 13-20, and 22-27 depend from base claims 1, 12, and 21, respectively and, hence, inherit all limitations of their base claim. Accordingly, Applicants respectfully submit that Marisetty does not anticipate claims 1-27.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 06-2380, under Order No. 08-2025, from which the undersigned is authorized to draw. The fee relative to the Request for Continued Examination is addressed in the Request as filed concurrently herewith.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Label No. EV482709143US in an envelope addressed to: M/S R.C.E., Commissioner for Patents, Alexandria, VA 22313.

Date of Deposit: September 14, 2005

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Respectfully submitted,

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